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Self-sensing cantilevers with integrated conductive coaxial tips for high-resolution electrical scanning probe metrology

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The lateral resolution of many electrical scanning probe techniques is limited by the spatial extent of the electrostatic potential profiles produced by their probes. Conventional unshielded conductive atomic force microscopy probes produce broad potential profiles. Shielded probes could offer higher resolution and easier data interpretation in the study of nanostructures. Electrical scanning probe techniques require a method of locating structures of interest, often by mapping surface topography. As the samples studied with these techniques are often photosensitive, the typical laser measurement of cantilever deflection can excite the sample, causing undesirable changes electrical properties. In this work, we present the design, fabrication, and characterization of probes that integrate coaxial tips for spatially sharp potential profiles with piezoresistors for self-contained, electrical displacement sensing. With the apex 100 nm above the sample surface, the electrostatic potential profile produced by our coaxial tips is more than 2 times narrower than that of unshielded tips with no long tails. In a scan bandwidth of 1 Hz–10 kHz, our probes have a displacement resolution of 2.9 Å at 293 K and 79 Å at 2 K, where the low-temperature performance is limited by amplifier noise. We show scanning gate microscopy images of a quantum point contact obtained with our probes, highlighting the improvement to lateral resolution resulting from the coaxial tip.

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I. INTRODUCTION

Building on the principles of atomic force microscopy (AFM), researchers have developed a wide range of electrical scanning probe techniques to measure and manipulate the local electronic properties of materials. These techniques include scanning gate microscopy, electrostatic force microscopy, and Kelvin probe force microscopy which together enable mapping of current flow, surface potential, and work function. Common to each of these techniques is the need for a conductive probe with a sharp tip that is used to produce an electrostatic potential perturbation at the sample. The affect of this perturbation on the sample or the probe itself is recorded as the probe is raster scanned to produce an image. For example, in scanning gate microscopy (SGM), the conductance through the sample is measured as the tip modulates energy barriers or backscatters current carriers. In this way, SGM has been used to map branched current flow in two-dimensional electron gases (2DEGs)¹–⁴ and to identify energy barriers in carbon nanotubes (CNTs).³–⁹ The lateral resolution of AFM is limited by the tip geometry, as features in the image plane are a spatial convolution between the tip and sample. Sharper tips (i.e., those that approach a spatial delta function) produce more accurate images of the sample. Similarly, the lateral resolution of electrical scanning probe techniques is limited by the spatial extent of the electrostatic potential profile produced by the conductive probe. Often, the shape of the potential profile is controlled by the tip shape. However, the method of fabricating the conductor also plays a role. Consider the most commonly used conductive probes, commercially available metal-coated AFM probes. Because the conductor blankets the entire cantilever and tip cone and is completely unshielded, it produces a broad potential profile. Thus, while these probes have been used to study nanostructures such as CNTs, the features in the resulting images often appear larger than the nanostructures themselves, blurring their true location and size. Furthermore, even when these probes are used to image mesoscale samples such as 2DEGs, non-trivial measurement techniques and data post-processing are often required to separate the data of interest from the background influence of the broad profile. To facilitate accurate, high-resolution electrical imaging of nanostructures, a tip capable of producing a spatially sharp electrostatic potential profile is needed.

Electrical scanning probe techniques require a means of locating structures of interest, typically accomplished by mapping surface topography. As the samples studied with these techniques are often photosensitive, the conventional laser measurement of cantilever deflection can excite the sample and cause undesirable changes electrical properties. At cryogenic temperatures, photoexcited carriers can take hours or days to relax. Thus, the ideal electrical scanning probe should have a built-in sensor that enables electrical

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readout of cantilever deflection. Self-sensing probes provide additional benefits including faster setup (no optical alignment required) and reduced system size, complexity, and cost.

Using a tip with a coaxial structure, it is possible to produce a highly localized potential perturbation. Such a tip consists of an inner conductor, insulator, and outer shield. At the tip apex, a small aperture in the shield allows electric field lines from the inner conductor to reach the sample. Coaxial tips were first explored for scanning near-field optical microscopy. However, these tips were rudimentary in construction. More recently, several microfabricated coaxial tips have been reported and some applied to electrical scanning probe techniques.

Self-sensing cantilevers have been demonstrated using capacitors, piezoelectrics, quartz tuning forks, and piezoresistors. Piezoresistors are attractive as sensors because they can be readily fabricated using CMOS-compatible processes, their resistance change can be detected with a simple Wheatstone bridge circuit, and they provide linear response to stress with large dynamic range (Ref. 33)). Researchers have continued to improve piezoresistive cantilevers by integrating actuators, enabling measurement of lateral forces, integrating on-chip signal conditioning, and optimizing force resolution.

In this paper, we present new scanning probes that integrate coaxial tips for spatially sharp electrostatic potential profiles with piezoresistive cantilevers for self-contained, electrical displacement sensing. Like commercial AFM probes, the probes are batch fabricated using standard semiconductor manufacturing methods. We describe the design, fabrication, and characterization of this new probe. We show scanning gate microscopy images of a quantum point contact obtained with our probes, highlighting the improvement to lateral resolution resulting from the coaxial tip.

II. DESIGN

Our scanning probe design is based on the results of a previously reported numerical optimizer and was adapted for displacement resolution and 4-leg cantilevers. Cantilever mechanical properties predicted by the optimizer, including spring constant and resonant frequency, were verified by finite element analysis (FEA) with COMSOL Multiphysics. We also used FEA to compare the electric field distributions produced by an unshielded tip and a coaxial tip, Figs. 1 and 2.

There are several differences between the current scanning probes and our previous design. First, the piezoresistor and inner conductor to the coaxial tip are n-type, formed by phosphorus diffusion into p-type silicon. We selected this process as it allows us to easily fabricate dopant profiles with high surface concentration and shallow junction depths. Second, we moved the compensation piezoresistor from the die, where it was not released, to a separate cantilever with the same geometry as the active cantilever. This more closely matches the environments of the two piezoresistors and improves rejection of common mode signals (e.g., fluctuations in ambient temperature) when differential readout is employed. Last, we included a design variation in which the silicon between electrical traces is removed to minimize leakage paths and better define piezoresistor geometry. This results in a cantilever with four legs as seen in Fig. 3. With less current leakage between n-type diffusions, sensitivity to tip displacement is improved and cross-talk between the coaxial tip and the piezoresistor is reduced. The numerical optimizer we used is written in Matlab and can calculate the performance of a user-specified design or, given an optimization goal (for example, minimize the resolvable force at the tip) and constraints (power consumption, bandwidth, etc.), can vary the parameters of an initial design to arrive at a more optimized probe. In this design, the optimized parameters were cantilever and piezoresistor geometries as well as doping time and temperature. The optimizer uses a recursive method to optimize and find the optimal displacement resolution while keeping the parameters within the defined design bounds. More details on the design and operation of the optimizer can be found in Ref. 39. We made the following enhancements to the code to enable optimization of n-type piezoresistive cantilevers for contact mode AFM.
displacement, given by the voltage force sensitivity as defined in Ref. 40. For contact added to ability to minimize mode AFM, where we are sensing tip displacements, we thus, the optimization goal was to minimize \( F_{\text{min}} \), the minimum resolvable force, given by

\[
F_{\text{min}} = \frac{V_{\text{noise}}}{S_{\text{FV}}},
\]

where \( V_{\text{noise}} \) is the root mean square noise voltage and \( S_{\text{FV}} \) is the voltage force sensitivity as defined in Ref. 40. For contact mode AFM, where we are sensing tip displacements, we added to ability to minimize \( d_{\text{min}} \), the minimum resolvable displacement, given by

\[
d_{\text{min}} = \frac{V_{\text{noise}}}{S_{dV}},
\]

where \( S_{dV} \) is the voltage displacement sensitivity. The sensitivities \( S_{\text{FV}} \) and \( S_{dV} \) are related by \( k \), the cantilever spring constant, such that \( S_{dV} = kS_{\text{FV}} \).

### B. Cantilevers with four legs

The code previously assumed a cantilever with uniform width. We modified the expression for \( SFV \), applicable for a quarter-active Wheatstone bridge readout circuit, for cantilevers with four legs

\[
S_{\text{FV}} = \frac{3(l_c - 0.5l_p)\pi t_{\text{max}}}{8 w_p^2} \gamma V_{\text{bridge}} \beta^*.
\]

Here, \( l_c \) and \( t_c \) are the length and thickness of the cantilever, \( l_p \) and \( w_p \) are the length and width of the piezoresistor (with equivalent dimensions for the legs), \( l_{\text{max}} \) is the maximum piezoresistance coefficient, \( V_{\text{bridge}} \) is the voltage across the bridge, and \( \gamma \) and \( \beta^* \) are the geometry and efficiency factors as defined in Ref. 40. In the denominator, we replaced \( w_c \), the width of the cantilever, with \( 4w_p \), the effective width at its root. To calculate \( S_{dV} \), we derived \( k \) for a cantilever with four legs

\[
k = \frac{E t_c^3}{4 \frac{l_p^4}{w_c} + l_p \left( \frac{1}{w_p} - \frac{4}{w_c} \right) \left( \frac{l_p^2}{2} - 3l_pl_p + 3l_p^2 \right)},
\]

where \( E \) is the elastic modulus of the cantilever material. Although the cantilever is made of silicon with silicon dioxide and aluminum thin films on top, a single \( E \) is a good approximation as the silicon layer is \( 40 \times \) thicker. To arrive at this expression, we equated the internal and external torques from a force at the tip, using a piecewise function for the cantilever moment of inertia corresponding to the regions with and without legs.

### C. Piezoresistance factor and dopant activation

To calculate \( \beta^* \) in (3), we need the relationship between piezoresistance factor and carrier concentration. Because our piezoresistors are n-type, we replaced the p-type relationship reported by Harley with the n-type relationship of Tufte and Stelzer. The code uses Tsai's model to predict phosphorus concentration profiles for a given diffusion time and temperature. Instead of assuming complete dopant ionization, we now convert the dopant concentration profiles into carrier concentration profiles using activation data from Fair and Tsai.

### D. Ambient temperature

As SGM is often performed at cryogenic temperatures, we now permit a user-specified ambient temperature instead of fixing it at 300K. Currently, changing the temperature only affects the calculation of Johnson noise. We are working on adding the temperature dependence of mobility and dopant activation.
E. Inactive resistance

The factor in (3) is the ratio of the active resistance of piezoresistor, specifically the resistance of the two longitudinal legs, to the total measured resistance. Previously, this factor was determined by FEA and entered into the code. Instead, we derived an expression for using an equivalent resistance model

\[ \gamma = \frac{2R_{\text{long}}}{R_{\text{loop}} + R_{\text{shunt}} + R_{\text{loop}}}, \]

(5)

where \( R_{\text{loop}} = 2R_{\text{long}} + R_{\text{trans}} + 2R_{c} \). \( R_{\text{long}} \) and \( R_{\text{trans}} \) are the longitudinal and transverse resistances of the piezoresistor, \( R_{\text{shunt}} \) is the effective resistance due to leakage between the piezoresistor legs and \( R_{c} \) is the contact resistance from the metal electrodes to the piezoresistor. The latter two resistances can be determined with test structures fabricated alongside the scanning probes. We assume that the resistance of the metal traces and wire bonds is negligible. If \( R_{\text{shunt}} \) is large, as is the case when the silicon between neighboring traces is removed, the fraction on the right of 5 approaches unity.

F. Tip offset

The code previously assumed that the cantilever is loaded at its free end. However, in the case of scanning probes, the sharp tip interacts with the sample. This tip is typically offset from the free end of the cantilever by a distance we define as \( l_{\text{offset}} \). To calculate the cantilever properties at the tip location, we replaced all occurrences of \( l_{c} \) with \( l_{c} - l_{\text{offset}} \). The design parameters and predicted performance of our scanning probes resulting from the optimizer with the enhancements discussed above are provided in (1). As the devices presented here are intended for room temperature operation, we specified an ambient temperature of 300 K. In addition, we restricted power dissipation in the piezoresistor to 2 mW to keep the cantilever self-heating below \( \approx 100^\circ \text{C} \). We selected a measurement bandwidth of 10 kHz (1 Hz–10 kHz) for reasonable scan times, and placed an upper bound of 10 N/m on the cantilever spring constant to minimize damage to the sample while scanning. To facilitate fabrication, we specified a minimum diffusion time \( t_{\text{diff}} \) of 15 min and a range for the diffusion temperature \( T_{\text{diff}} \) of 1073 K–1173 K. The remaining parameters were determined by the optimizer.

III. FABRICATION

We fabricated the scanning probes using a batch process that produces >100 devices per wafer. We then opened the lateral and insulator at the apex of each tip, exposing the inner conductor, using focused ion beam (FIB) milling. These methods are described in detail below.

A. Batch Fabrication of cantilever probes

We fabricated the scanning probes from 4-in. (100) double-side polished p-type silicon-on-insulator (SOI) wafers with device, buried oxide (BOX), and handle layer thicknesses of 6.5 μm, 0.5 μm, and 400 μm and a nominal resistivity of 1–5 Ω cm. Our process is illustrated in Figure 4. We first etched alignment marks in the device layer silicon with CHF₃/O₂ plasma. Our next sequence of steps produced sharp silicon tips. We oxidized the wafers at 1100 °C for 39 min in pyrogenic steam to grow a 5000 Å hard mask. We patterned the oxide into discs with CHF₃/O₂ plasma. We etched the unmasked silicon isotropically in SF₆ plasma, undercutting the discs to form conical tip precursors. We observed the tops of the precursors through the transparent discs, and stopped the etching when they could no longer be resolved with an optical microscope. We chose a disc diameter of 4 μm to yield tip heights of ~3 μm with this etch recipe. We stripped the masks in 6:1 buffered oxide etch (BOE) and oxidized the wafers at 900 °C for 43 min in steam. At temperatures below 950 °C, the build-up of stress inhibits oxidation at regions of high curvature. Thus, the oxidation sharpened the precursors into final tips. Next, we created the piezoresistors and inner conductors by phosphorus diffusion. We used the 1000 Å of oxide grown during the sharpening process as a hard mask, patterning it in 6:1 BOE. We avoided dry etching in order to maintain tip sharpness. We

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**FIG. 4.** Batch process used to fabricate our cantilever probes from silicon-on-insulator wafers: (a) Etch alignment marks, grow thermal oxide, and pattern oxide into discs at the tip locations. Etch device layer Si in SF₆ plasma, undercutting the discs to form tip precursors. Remove discs. (b) Grow thermal oxide to sharpen tips, then pattern oxide and perform phosphorus diffusion to create piezoresistors and inner conductors. (c) Strip oxide mask and deposit low-temperature oxide to form insulator. Open contacts to diffusions. (d) Sputter and pattern Al into outer shields and bond pads. (e) Define and (f) release cantilevers with deep reactive ion etching. Clear buried oxide in CHF₃/O₂ plasma.
performed the diffusion at 850 °C for 15 min (parameters calculated by the numerical optimizer) in a POCl3 ambient. We stripped the phosphosilicate glass deposited during the diffusion and the oxide mask in 6:1 BOE.

To passivate the piezoresistors and create the insulator for the coaxial tips, we deposited 400 Å of low-temperature oxide (LTO) at 400 °C. This film thickness withstands 10 V between the inner conductor and outer shield before electrical breakdown but does not round the tip apex significantly. We used LTO instead of thermal oxide to mitigate dopant diffusion which would degrade piezoresistor performance. We etched contact vias to the n-type silicon using 20:1 BOE and immediately sputtered 400 Å of aluminum. We patterned the metal into the outer shield for the coaxial tips and the bond pads for the piezoresistors and the inner conductors with AL-11 wet etchant at 40 °C. Again, we selected the film thickness to minimize tip rounding.

We defined the cantilevers and die outlines by etching the device layer silicon in HBr/Cl2 plasma, stopping on the BOX. To release the cantilevers, we etched through the handle layer with deep reactive ion etching (DRIE), again stopping on the BOX, then cleared the BOX in CHF3/O2 plasma. During this process, the frontside of the wafer was protected with 7 μm of SPR220–7 resist. Finally, we cleaned the wafers in PRS-1000 at 40 °C. Scanning electron microscope (SEM) images of a completed device are presented in Figure 5.

**B. Opening the coaxial tip**

We used FIB milling to obtain small, controlled apertures at the tip apex. We performed the milling with an FEI Strata 235DB dual-beam FIB/SEM in which the electron beam (E-beam) and ion-beam (I-beam) are coincident on the sample and separated by 52°. We aligned the I-beam parallel to the cantilever and opened the tip from the side using a rectangular milling pattern, as shown in Figure 6. We drew the pattern such that one edge overlaps the tip apex. We set the I-beam to mill the rectangle one line at a time, ending at the overlapping edge, instead of raster scanning the entire pattern for the duration of the etching. The line-by-line approach is known as a cleaning cross-section and produces a high-quality surface at the end of the tip. We used a 1 pA Ga⁺ ion current to achieve a slow milling rate and to limit damage to the probe while imaging. We milled until clear contrast could be observed between the exposed inner conductor and outer shield in E-beam images. With this method, we could repeatably produce apertures of 30 nm in radius. SEM images of a tip before and after milling are shown in Figure 7.

**IV. RESULTS AND DISCUSSION**

Figure 8 shows a representative topography scan using our tips. We measured the vertical displacement resolution of our scanning probes at 293 K and 2 K for the corresponding designs. At room-T, we mounted the probe in a Witec Alpha300A AFM system and placed the active and compensation piezoresistors in a Wheatstone bridge configuration.
with two matched metal-film resistors. We connected the output of the bridge to a Texas Instruments INA103 amplifier with $1000 \times$ gain. For low-T measurements, we used a home-built scanning system contained within a top-loading $^3$He cryostat. The readout circuit consisted of a Wheatstone bridge followed by two Stanford Research Systems SR560 amplifiers in series, with gains of $100 \times$ and $500 \times$. The compensation piezoresistor was not used because the temperature in the cryostat is well controlled. During operation, the three matched resistors in the bridge are at the same temperature as the probe; while the amplifiers remain at room-T. In either systems, the probes were mounted at a $12^\circ$ angle with respect to the sample. At both temperatures, we first measured the voltage noise with the tip out of contact and then measured the output voltage as the cantilever was deflected with a hard sample, giving displacement sensitivity. We calculated displacement resolution by dividing the integrated noise in 1 Hz–10 kHz by the sensitivity. We also measured the resonant frequency by vibrating the probes with an external piezoelectric actuator and identifying a sharp peak in the output voltage as we swept the excitation frequency. Our results are summarized in Tables I and II, where the predicted values have been updated to reflect actual probe geometry as measured by SEM ($l_c = 174.5 \mu m$ and $t_c = 2.5 \mu m$).

At room-T, the scanning probe is able to resolve displacements of 2.94 Å. The predicted and measured values all agree within 5% with a resolution variation over measured devices of 5%. At low-T, the measured displacement sensitivity is $\sim 18\%$ lower than predicted. We calculated the predicted sensitivity using room-T values for the piezoresistive coefficient $\pi_1$ as we did not have data for n-type diffusions at 2 K. Thus, the discrepancy between the measured and predicted values can be explained by the variation of $\pi_1$ with temperature.

### Table I. Design parameters and predicted AFM performance of scanning probes. Measurements bandwidth is 1 Hz–10 kHz.

<table>
<thead>
<tr>
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<th>Room-T</th>
<th>Low-T</th>
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</thead>
<tbody>
<tr>
<td>Temperature (K)</td>
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<tr>
<td>Bridge voltage (V)</td>
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<tr>
<td>Cantilever dimensions</td>
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<tr>
<td></td>
<td>$w_c$ ($\mu m$)</td>
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</tr>
<tr>
<td></td>
<td>$t_c$ ($\mu m$)</td>
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<tr>
<td>Piezoresistor dimensions</td>
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<td></td>
<td>$w_p$ ($\mu m$)</td>
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</tr>
<tr>
<td>Spring constant (N/m)</td>
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<tr>
<td>Resonant frequency (kHz)</td>
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<td>154</td>
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<td>Power dissipation ($\mu W$)</td>
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<tr>
<td>Displacement sensitivity (kV/m)</td>
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<tr>
<td>Johnson noise (nV/$\sqrt{Hz}$)</td>
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<td>4</td>
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<tr>
<td>Hooge noise (nV/$\sqrt{Hz}$) at 10 Hz</td>
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<tr>
<td>Total noise (nV)</td>
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<tr>
<td>Displacement resolution (Å)</td>
<td>1.63</td>
<td>14.2</td>
</tr>
</tbody>
</table>

### Table II. AFM performance of two fabricated scanning probes. Two separate designs are presented optimized for room or low temperature. Boldface values are measured, others are predicted. Measurements bandwidth is 1 Hz–10 kHz.

<table>
<thead>
<tr>
<th></th>
<th>Room-T</th>
<th>Low-T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature (K)</td>
<td>293</td>
<td>2</td>
</tr>
<tr>
<td>Bridge voltage (V)</td>
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<td>0.2</td>
</tr>
<tr>
<td>Spring constant (N/m)</td>
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<td>Resonant frequency (kHz)</td>
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<td>114</td>
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<td></td>
<td>100</td>
<td>103</td>
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<tr>
<td>Displacement sensitivity (kV/m)</td>
<td>2.00</td>
<td>0.146</td>
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<tr>
<td>Total noise (nV)</td>
<td>587</td>
<td>1150</td>
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<tr>
<td></td>
<td>581</td>
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<tr>
<td>Displacement resolution (Å)</td>
<td>2.94</td>
<td>78.8</td>
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<td></td>
<td>2.86</td>
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</table>
In Figure 9, we plot \( \pi_l \) for n-type diffusions with different surface concentrations \( n_s \) down to 77 K, taken from Tufte and Stelzer.\(^{45} \) Because the carrier concentration varies with depth in diffused piezoresistors, the \( \pi_l \) values presented here are conductivity-weighted averages over the thickness. We see that below \( \sim 100 \) K, \( \pi_l \) decreases with temperature. The \( \pi_l \) values extracted from our piezoresistors (\( n_s = 1.3 \times 10^{20} \) cm\(^{-3} \), verified by spreading resistance analysis) show good agreement with the existing data. We also see that the measured noise is \( 2.7 \times \) larger than predicted. At low-T operating conditions, the two main sources of noise from the piezoresistor are small (\( V_{\|}^2 J / T \) and \( V_{\|}^2 H / V^2 \) bridge). Total noise is determined by the amplifier noise floor. We verified that the total noise did not change when the inputs of the first-stage amplifier were disconnected from the bridge and grounded. Thus, although the scanning probe is only able to resolve displacements of 78.8 \( \text{Å} \), the resolution is limited by the amplifier. Switching from the SR560 (4 nV/\( \sqrt{\text{Hz}} \) at 1 kHz) to the INA103 (1 nV/\( \sqrt{\text{Hz}} \) at 1 kHz) should allow displacements of 7.19 \( \text{Å} \) to be resolved.

We measured the electrostatic potential profile produced by our coaxial tips using a quantum point contact. At 2 K, we first obtained a plot of conductance \( G_{\|} \) through the QPC versus voltage \( V_G \). Temperature. In Figure 9, we plot \( \pi_l \) for n-type diffusions with different surface concentrations \( n_s \) down to 77 K, taken from Tufte and Stelzer.\(^{45} \) Because the carrier concentration varies with depth in diffused piezoresistors, the \( \pi_l \) values presented here are conductivity-weighted averages over the thickness. We see that below \( \sim 100 \) K, \( \pi_l \) decreases with temperature. The \( \pi_l \) values extracted from our piezoresistors (\( n_s = 1.3 \times 10^{20} \) cm\(^{-3} \), verified by spreading resistance analysis) show good agreement with the existing data. We also see that the measured noise is \( 2.7 \times \) larger than predicted. At low-T operating conditions, the two main sources of noise from the piezoresistor are small (\( V_{\|}^2 J / T \) and \( V_{\|}^2 H / V^2 \) bridge). Total noise is determined by the amplifier noise floor. We verified that the total noise did not change when the inputs of the first-stage amplifier were disconnected from the bridge and grounded. Thus, although the scanning probe is only able to resolve displacements of 78.8 \( \text{Å} \), the resolution is limited by the amplifier. Switching from the SR560 (4 nV/\( \sqrt{\text{Hz}} \) at 1 kHz) to the INA103 (1 nV/\( \sqrt{\text{Hz}} \) at 1 kHz) should allow displacements of 7.19 \( \text{Å} \) to be resolved. We measured the electrostatic potential profile produced by our coaxial tips using a quantum point contact. At 2 K, we first obtained a plot of conductance \( G_{\|} \) through the QPC versus voltage \( V_G \).
on the surface gates. To measure $G_{ds}$, we applied a small AC voltage (~4 $\mu$V) across the ohmic contacts and recorded the resulting current using a DL 1211 current preamplifier and an EG&G 124A lock-in amplifier. Then, we selected $V_G$ such that the QPC was between the first and second conductance plateaus. In this region, $dG_{ds}/dV_G$ is approximately linear. When the tip is placed in proximity to the QPC, it acts as a third gate and the tip potential modulate the channel conductance. Thus, by recording $G_{ds}$ as a third gate and the tip potential, we can independently address the inner conductor and the 2DEG below, modulating the conductance plateaus. As the probe is scanned above the QPC, a spatial map of the tip potential can be obtained.

In Figure 10, we present 8 $\mu$m $\times$ 8 $\mu$m maps of $G_{ds}$ acquired at a lift height of 100 nm above the semiconductor surface as in Figure 11. We set $V_G = -0.730$ V, yielding a nominal $G_{ds} = 2.56$ $e^2/h$. We varied the inner conductor voltage $V_{ic}$ from $-2$ V to $+2$ V in steps of 2 V and the outer shield voltage $V_{sh}$ from $-1$ V to $+1$ V in steps of 1 V, producing a $3 \times 3$ array of maps (see linecuts in Figure 12). The maps show that we can independently address the inner conductor and outer shield and that both are capable of gating the QPC. Qualitatively, we see that by tuning $V_{sh}$, we can narrow the perturbation created by the inner conductor and eliminate the slow decay in potential that is characteristic of an unshielded tip. Consider the bottom row of images where $V_{ic} = -2$ V. When $V_{sh} = -1$ V, $G_{ds}$ is suppressed in the entire scan window. Even when the tip is several microns from the QPC, the long range fields from the inner conductor and shield result in a negative $\Delta G_{ds}$. When $V_{sh} = 0$ V, the region of strong suppression from the inner conductor is reduced. Furthermore, with this biasing, when the tip is not directly above the QPC, $G_{ds}$ returns to its nominal value. Finally, when $V_{sh} = +1$ V, the perturbation produced by the inner conductor is even narrower. However, the potential on the shield now enhances $G_{ds}$.

Two surprising features are apparent in the maps. First, when $V_{ic}$ and $V_{sh}$ are 0 V, we intuitively expect that the tip will have no effect on QPC conductance. However, centered above the QPC, we see a small region of suppression surrounded by a halo of enhancement. Poggio et al. also observed a change in $G_{ds}$ in response to a grounded cantilever when they used a QPC as a displacement sensor. The authors hypothesized that the modulation of conductance was a result of trapped charge on the cantilever or differences in work function between the cantilever and sample materials. Here, we believe the latter explanation is valid. By tuning the $V_{ic}$ and $V_{sh}$, we can null the differences in work function and minimize the tip effect. For example, the halo is caused by the work function difference between the Al
shield and the AlGaAs/GaAs heterostructure. It is eliminated when we set $V_{sh} = -0.6$ V. The same voltage was reported by other researchers to null the work function difference between the Al island of a single-electron transistor scanning electrometer and an AlGaAs/GaAs heterostructure. The map of $G_{ds}$ tells us that the work function difference between the n-type Si inner conductor and the heterostructure has the opposite polarity of that between the Al outer shield and the heterostructure. In general, for SGM imaging with the coaxial tip, $V_{sh}$ should be tuned to null the work function difference between the outer shield and the sample such that the perturbation to the sample results strictly from the inner conductor.

Second, we see that the electrostatic potential profile from the tip appears elliptical instead of circular, with the long axis of the ellipse perpendicular to the surface gates. The QPC does not sample the tip potential at a single point in space. It responds to the potential in a nearby volume, which can be represented by a point spread function (PSF). The PSF sets the spatial resolution of QPC when it is used as a sensor. The maps of $G_{ds}$ are convolutions of the tip potential profile with the PSF. The shape of the resulting convolution is controlled by the broader of these two inputs. From our modeling, we expect that the FWHM of the potential profile produced by the coaxial tip is below the spatial resolution of the QPC, which is determined primarily by the channel width (300 nm). Thus, when the QPC is used to measure this profile, the map of $G_{ds}$ takes the shape of the PSF.

To calculate the FWHM of the convolution, which gives an upper bound on the FWHM of the tip potential profile, we considered maps of $G_{ds}$ with $V_{sh} = -0.6$ V. We subtracted the map with $V_{ke} = 0$ V from the map with $V_{ke} = -2$ V to eliminate the effect of work function differences and measured the FWHM of the result. Because the convolution is elliptical, we measured the FWHM in the x and y axes, yielding 350 nm and 240 nm, respectively. As expected, the FWHM values roughly correspond to the QPC channel width.

In Figure 13, we showed that the FWHM of the perturbation induced by an unshielded tip at $h_{lin} = 100$ nm is 560 nm. Using the QPC, we demonstrated that the FWHM of the potential profile coaxial tip at the same lift height is ≤240 nm. Thus, under these conditions, our coaxial tips improve the lateral resolution of SGM by ≥2.3×.

V. CONCLUSIONS

Scanning gate microscopy enables measurement of local current flow, carrier density, and potential barriers, but the lateral resolution of the technique has been limited by existing probes. We have demonstrated a new scanning probe that integrates a coaxial tip on a piezoresistive cantilever. By shielding the inner conductor up to the tip apex, the coaxial tip minimizes stray capacitance and produces tightly confined potential profiles. The piezoresistor provides self-sensing capability, allowing cantilever deflection to be measured electrically, without the traditional optical lever setup that can disturb photosensitive samples. We designed the piezoresistive cantilevers with the aid of a numerical optimizer and used finite element analysis to compare the electrostatic potential profiles from unshielded and coaxial tips. We showed that lift height and shield opening radius have the largest effect on profile width. We developed a 7-mask process to fabricate scanning probes with both a piezoresistor and a coaxial tip. We used FIB milling to open the shield metal at the tip apex. The smallest apertures we produced were ~30 nm in radius. We characterized the AFM performance of the probes by measuring the total system noise with the tip out of contact and then recording the readout circuit output while deflecting the cantilever with a hard sample to
calculate displacement sensitivity. The probes can self-sense tip displacements of 2.9 Å at 293 K and 79 Å at 2 K in a 10 kHz bandwidth, where the low-T performance is limited by amplifier noise. Finally, we imaged the potential profiles produced by the coaxial tips using a quantum point contact. At a lift height of 100 nm, the coaxial tips produce profiles that are $\geq 2.3 \times$ narrower than those of unshielded tips. We are currently using our self-sensing coaxial-tip probes to investigate carbon nanotube field effect transistors.

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